UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/813,296 | 03/30/2004 | Gary A. Kinstler | BOI - 0346US | 4531 |

60483 7590 06/30/2008

LEE & HAYES, PLLC
421 W. RIVERSIDE AVE.
SUITE 500
SPOKANE, WA 99201

| EXAMINER | |
|---|---|
| YUEN, KAN | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2616 | |

| MAIL DATE | DELIVERY MODE |
|---|---|
| 06/30/2008 | PAPER |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/813,296 | KINSTLER, GARY A. | |
| | Examiner | Art Unit | |
| | KAN YUEN | 2616 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-27,29,31 and 33-36* is/are rejected.

7)☒ Claim(s) *12,28,30 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/7/2008 has been entered.

***Response to Arguments***

2. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Objections***

3. Claims 1-36 are objected to because of the following informalities:

4. In claim 1, line 13, the term "busses" should be spelled as "buses". Applicant is suggested to fix this minor issue in the rest of the claims. Appropriate correction is required.

***Claim Rejections - 35 USC § 103***

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 5-7, 11, 21, 25, 26, 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), and Lu et al. (Pat No.: 7269133), and further in view of Fee et al. (Pat No.: 5485576).

For claim 1, Kramer et al. disclosed the method of transmitting periodically a first message from one of the plurality of nodes to another of the nodes on a first of the plurality of busses of the network **(Kramer et al. see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of modules (14, 16, 18, 20) coupling with each other with 2 buses (10, 12). Status message or the first message is being transferred from one module 14 to module 16 periodically. Each module has two identical units such as A0, B0, A1, B1, A2, and B2. Each bus 10 and 12 are connected to both identical unit of each module for redundancy reason;

determining whether the first message was received by the other of the nodes on the first bus; and when it is determined that the first message was not received by the other of the nodes, transmitting a recovery command to the other of the nodes on a second of the plurality of busses **(Kramer et al. see column 3, lines 15-35, see column 6, lines 35-67, and see column 7, lines 1-15, and see fig. 1).** After fault detection, the transmitting module will generate a relevant message or the recovery message to the module again using any of the 2 buses (10, 12) or the second bus. Since all bus subscribers transmit message independently, the bus are different;

each node of the bus interface circuit including a physical layer controller that sends and receives data on one of the plurality of buses **(Kramer et al. column 5, lines 45-67, column 6, lines 1-20).** Each bus subscribers comprises two controller modules 56-62 for transmitting and receiving data on plurality of buses.

However, Kramer et al. do not teach the recovery command that is configured to cause the other of the nodes to clear a latch-up error in a bus interface circuit that operatively connects the other of the nodes to the first bus and a link layer controller that encodes and decodes the data.

Lu et al. from the same or similar fields of endeavor teaches the recovery command is configured to cause the other of the nodes to clear a latch-up error in a bus interface circuit that operatively connects the other of the nodes to the first bus **(Lu et al. see column 11, lines 34-45, and see fig. 1 and fig. 2).** Shown in fig. 1, where HA system is denoted 10, and there are active MCP unit 11 and backup MCP unit 12. When the backup receives the first IS-IS PDU on the interface, it sends a

synchronization message or the recovery command to active MCP, and clear its own synchronization flag. When active MCP receives the message, it also clears the synch flag, and therefore the synchronization flag can be considered as the latch-up error. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Lu et al. in the network of Kramer et al. The motivation for using the feature as taught by Lu et al. in the network of Kramer et al. being that it provides reliability in each node.

However, Kramer et al. and Lu et al. both do not teach the link layer controller that encodes and decodes the data.

Fee et al. from the same or similar fields of endeavor teaches the link layer controller that encodes and decodes the data **(Fee et al. fig. 4, 106, column 6, lines 20-45).** The microprocessor 70 comprises a message encode and decode 106.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Fee et al. in the network of Kramer et al. and Lu et al. The motivation for using the feature as taught by Fee et al. in the network of Kramer et al. and Lu et al. being that it provides security in the network.

Regarding claim 5, Kramer et al. disclosed the feature of transmitting periodically the first message further comprises transmitting the first message on each of the plurality of busses **(Kramer et al. see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of modules (14, 16, 18, 20) coupling with each other with 2 buses (10, 12). Status or the first message is being transferred from one module 14 to module 16 periodically.

Regarding claim 6, Kramer et al. disclosed the feature of transmitting periodically the first message further comprises transmitting the first message from the one node to each of the other nodes **(Kramer et al. see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of modules (14, 16, 18, 20) coupling with each other with 2 buses (10, 12). Status or the first message is being transferred from one module 14 to all modules 16, 18, and 20 periodically.

Regarding claim 7, Kramer et al. disclosed the feature of the nodes transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame **(Kramer et al. see column 7, lines 49-55).** As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 11, Kramer et al. disclosed the feature of the second bus is a different type of bus than the first bus **(Kramer et al. see column 3, lines 15-35)** Since all bus subscribers transmit message independently, the bus are different.

Claim 21 is rejected similar to claim 1.

Regarding claim 25, Kramer et al. disclosed the feature of transmitting periodically the first message further comprises transmitting the first message from the one node to each of the other nodes **(Kramer et al. see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of

modules (14, 16, 18, 20) coupling with each other with 2 buses (10, 12). Status or the first message is being transferred from one module 14 to module 16 periodically.

Regarding claim 26, Kramer et al. disclosed the feature of the nodes transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame **(Kramer et al. see column 7, lines 49-55).** As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 29, Kramer et al. disclosed the feature of the second bus is a different type of bus than the first bus **(Kramer et al. see column 3, lines 15-35).** Since all bus subscribers transmit message independently, the bus are different.

8. Claims 2 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), and Fee et al. (Pat No.: 5485576), as applied to claim 1 above, and further in view of Qian et al. (Pub No.: 2005/0030926).

For claims 2, and 22 Kramer et al. Fee et al. and Lu et al. disclosed all the subject matter of the claimed invention with the exception of the other of the nodes cycles power to a bus interface circuit operatively connecting the other node to the first bus in response to the recovery command. Qian et al. from the same or similar fields of

endeavor teaches the feature of the other of the nodes cycles power to a bus interface circuit operatively connecting the other node to the first bus in response to the recovery command **(see paragraph 0008, lines 1-25).** As shown, the power levels of the R-SPICH channel or the first bus link is made available based on the data rate received on the reverse channel or second bus link. Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Qian et al. in the network of Kramer et al. Fee et al. and Lu et al. The motivation for using the feature as taught by Qian et al. in the network of Kramer et al. Fee et al. and Lu et al. being that the received data rate can re-establish the link to make it available for utilization.

9. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), Fee et al. (Pat No.: 5485576), and Qian et al. (Pub No.: 2005/0030926), as applied to claim 2 above, and further in view of Kenkare (Pub No.: 2005/0013319).

For claim 3, Kramer et al., Lu et al., Fee et al. and Qian et al. disclosed all the subject matter of the claimed invention with the exception of the link layer controller is further configured to handle frame synchronization for the data. Kenkare from the same or similar fields of endeavor teaches the feature of the link layer controller is further configured to handle frame synchronization for the data **(Kenkare paragraph 0008).** Thus, it would have been obvious to the person of ordinary skill in the art at the time of

the invention to use the feature as taught by Kenkare in the network of Kramer et al. Fee et al. Lu et al, and Qian et al. The motivation for using the feature as taught by Kenkare in the network of Kramer et al. Fee et al. Lu et al, and Qian et al. being that the controller provides compatibility to other nodes.

10. Claims 4, 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), Fee et al. (Pat No.: 5485576), and Qian et al. (Pub No.: 2005/0030926), as applied to claim 2 above, and further in view of Reeves et al. (Pub No.: 2005/0162882).

For claims 4, 24 Kramer et al., Lu et al., Fee et al. and Qian et al. disclosed all the subject matter of the claimed invention with the exception of each node of the bus interface circuit is operatively connected to a data processing computer. Reeves from the same or similar fields of endeavor teaches the feature of each node of the bus interface circuit is operatively connected to a data processing computer **(Reeves et al. fig. 2, paragraph 0027).** Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Reeves et al. in the network of Kramer et al. Fee et al. Lu et al, and Qian et al. The motivation for using the feature as taught by Reeves et al. in the network of Kramer et al. Fee et al. Lu et al, and Qian et al. being that enhances the processing time.

11. Claims 8, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), and Fee et al. (Pat No.: 5485576), as applied to claim 1 above, and further in view of Engels et al. (Pub No.: 2004/0213174).

Regarding claims 8, 27 Kramer et al., Lu et al., Fee et al. disclosed all the subject matter of the claimed invention with the exception of the nodes transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame. Engels et al. from the same or similar fields of endeavor teaches the feature of the nodes transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is at least one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once each minor frame **(Engels et al. see paragraph 0028, lines 1-4).** The uplink frame, which includes plurality of mini time slot frames, is allocated for data transmission in each individual slot frame. The data can be any kind of messages.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Engels et al. in the network of Kramer et al. Fee et al. and Lu et al. The motivation for using the feature as taught by Engels et al. in the network of Kramer et al. Fee et al. and Lu et al. being that the minor frames can be transmitted without major delay.

12. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), and Fee et al. (Pat No.: 5485576), as applied to claim 1 above, and further in view of Ishida (Pat No.: 5170473).

Regarding claim 9, Kramer et al., Lu et al., Fee et al. disclosed all the subject matter of the claimed invention with the exception of determining whether the first message was received comprises sending a second message to the other of the nodes on the first bus if the first message is not received by the other of the nodes and determining whether the second message was received by the other of the nodes. Ishida from the same or similar fields of endeavor teaches the feature of determining whether the first message was received comprises sending a second message to the other of the nodes on the first bus if the first message is not received by the other of the nodes and determining whether the second message was received by the other of the nodes **(Ishida see column 4, lines 65-68, and see column 5, lines 1-5).** As shown, the signal is transmitted via the same path, which determines which CPU will receive the data. Therefore, we can interpret that the signal is sent on the same path as the previous path.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Ishida in the network of Kramer et al. Fee et al. and Lu et al. The motivation for using the feature as taught by Ishida in the network of Kramer et al. Fee et al. and Lu et al. being that the signal provides redundancy for determining if the path is working.

13. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), and Fee et al. (Pat No.: 5485576), as applied to claim 1 above, and further in view of Kim (Pat No.: 6064554).

For claim 10, Kramer et al., Lu et al., Fee et al. disclosed all the subject matter of the claimed invention with the exception of detecting a current surge in a bus interface circuit operatively connecting the one node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit. Kim et al. from the same or similar fields of endeavor teaches the feature of detecting a current surge in a bus interface circuit operatively connecting the one node to the first bus; and cycling power to the bus interface circuit in response to detecting the current surge in the bus interface circuit **(Kim et al. see column 2, lines 13-40).** The power unit is couple to the over-current or current surge detector.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Kim in the network of Kramer et al. Fee et al. and Lu et al. The motivation for using the feature as taught by Kim in the network of Kramer et al. Fee et al. and Lu et al. being that the over-current detection can provide protections to system cause by power outrage.

14. Claims 13, 14, 16, 17, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), and Ohyama (Pat No.: 4794595), and further in view of Fee et al. (Pat No.: 5485576).

For claim 13, Kramer et al. disclosed the method of a network having a plurality of busses; a plurality of nodes operatively connected to the plurality of busses of the network; means for transmitting periodically a first message from one of the plurality of nodes to another of the nodes on a first of the plurality of busses of the network **(see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of modules (14, 16, 18, 20) coupling with each other with 2 buses (10, 12). Status message or the first message is being transferred from one module 14 to module 16 periodically. Each module has two identical units such as A0, B0, A1, B1, A2, and B2. Each bus 10 and 12 are connected to both identical unit of each module for redundancy reason;

means for determining whether the first message was received by the other of the nodes on the first bus; and means for transmitting a recovery command associated with the first bus to the other of the nodes on a second of the plurality of busses in response to determining that the first message was not received by the other of the nodes **(see column 6, lines 35-67, and see column 7, lines 1-15, and lines 49-65 and see fig. 1).** After fault detection, the transmitting module will generate a relevant message or the recovery message to the module again using the 2 buses (10, 12) or the second bus. Since all bus subscribers transmit message independently, the bus are different.

However, Kramer et al. are silent on the nodes comprises a bus interface circuit operatively connecting the other node to the first bus, the bus interface circuit including a physical layer controller that sends and receives data on one of the plurality of buses; and a link layer controller and a means for interrupting power to the bus interface circuit and the means for interrupting power is configured to at least interrupt a current flow from the link layer controller to the physical layer controller in response to the recovery command; a link layer controller that encodes and decodes the data.

Ohyama from the same or similar fields of endeavor teaches the features of wherein the other of the nodes comprises a bus interface circuit **(Ohyama see fig. 4 DCE 7)** DCE is the data circuit terminal or the bus interface circuit; operatively connecting the other node to the first bus, the bus interface circuit including a physical layer controller that sends and receives data on one of the plurality of buses; and

a link layer controller **(see fig. 4, DCE 7).** The DCE comprises two ports where the first port or the physical layer controller supplies the L1 signal, and the second port or the link layer controller supplies the L2 signal; and

a means for interrupting power to the bus interface circuit (see fig. 4, DCE Main Part). The Main Part can be considered as the interrupting power unit; and the means for interrupting power is configured to at least interrupt a current flow from the link layer controller to the physical layer controller in response to the recovery command **(Ohyama see column 4, lines 11-15).** The current flowing between L1 and L2 may be interrupted by flickering the switch 19 depending on the On and Off state of a signal, wherein the signal can be the recovery command.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Ohyama in the network of Kramer et al. The motivation for using the feature as taught by Ohyama in the network of Kramer et al. being that it provides reliability in the network.

However, Kramer et al. and Ohyama both do not teach the link layer controller that encodes and decodes the data. Fee et al. from the same or similar fields of endeavor teaches the link layer controller that encodes and decodes the data **(Fee et al. fig. 4, 106, column 6, lines 20-45).** The microprocessor 70 comprises a message encode and decode 106.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Fee et al. in the network of Kramer et al. and Ohyama. The motivation for using the feature as taught by Fee et al. in the network of Kramer et al. and Ohyama being that the over-current detection can provide protections to system cause by power outrage.

Regarding claim 14, Ohyama disclosed the feature of the other of the nodes comprises: a means for receiving the recovery command, the means for receiving the recovery command configured to cause the means for interrupting power to interrupt current flow in response to the recovery command **(Ohyama see column 4, lines 11-15).** The current flowing between L1 and L2 may be interrupted by flickering the switch 19 depending on the On and Off state of a signal, wherein the signal can be the recovery command.

Regarding claim 16, Kramer et al. disclosed the feature of the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, and the first message is transmitted once in each frame **(Kramer et al. see column 7, lines 49-55).** As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 17, Kramer et al. disclosed the feature of the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame **(Kramer et al. see column 7, lines 49-55).** As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 19, Kramer et al. disclosed the feature of the second bus is a different type of bus than the first bus **(Kramer et al. see column 3, lines 15-35)** Since all bus subscribers transmit message independently, the bus are different.

Regarding claim 20, Ohyama disclosed the feature of for interrupting power flow is further configured to interrupt a current flow from a power bus to the physical layer controller in response to the recovery command **(Ohyama see column 4, lines 11-15).** The current flowing between L1 and L2 may be interrupted by flickering the switch 19

depending on the On and Off state of a signal, wherein the signal can be the recovery command.

15. Claims 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Ohyama (Pat No.: 4794595), and Fee et al. (Pat No.: 5485576), as applied to claim14 above, and further in view of Kim (Pat No.: 6064554).

For claim 15, Kramer et al. Ohyama and Fee et al. disclosed all the subject matter of the claimed invention with the exception of means for detecting a current surge in the bus interface circuit operatively connecting the other node to the first bus; and means for reporting the current surge in the bus interface circuit to the one node on the second bus. Kim from the same or similar fields of endeavor teaches the features of means for detecting a current surge in the bus interface circuit operatively connecting the other node to the first bus; and means for reporting the current surge in the bus interface circuit to the one node on the second bus **(Kim see column 3, lines 52-67, and see column 4, lines 1-3).** As shown, the detected current is transmitting to the USB controller 100.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the features as taught by Kim in the network of Kramer et al. Fee et al. and Ohyama. The motivation for using the features as taught by Kim in the

network of Kramer et al. Fee et al. and Ohyama being that the over-current detection can provide protections to system cause by power outrage.

Regarding claim 18, Kim disclosed the feature of the one node comprises: a bus interface circuit operatively connecting the one node to the first bus; means for detecting a current surge in the bus interface circuit; and means for cycling power to the bus interface circuit in response to detecting the current surge **(Kim et al. see column 2, lines 13-40).** The power unit is couple to the current detector.

16. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Lu et al. (Pat No.: 7269133), and Fee et al. (Pat No.: 5485576), and Qian et al. (Pub No.: 2005/0030926) as applied to claim 22 above, and further in view of Fukunaga et al. (Pub No.: 20060002314).

For claim 23, Kramer et al. Lu et al. and Fee et al. disclosed all the subject matter of the claimed invention with the exception of the physical layer controller is further configured to initialize and arbitrate communication on the one of the plurality of buses. Fukunaga et al. from the same or similar fields of endeavor teaches the feature of the physical layer controller is further configured to initialize and arbitrate communication on the one of the plurality of buses **(Fukunaga et al. paragraph 0245).** Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Fukunaga et al. in the network of Kramer et al. Fee et al. and

Lu et al. The motivation for using the feature as taught by Fukunaga et al. in the network of Kramer et al. Fee et al. and Lu et al. being that it provides reliability in the network.

17. Claims 31, 33, 34, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Ohyama (Pat No.: 4794595), and further in view of Fukunaga et al. (Pub No.: 20060002314).

Regarding claim 31 Kramer et al. disclosed a plurality of network interface cards operatively configured to connect to a network having a plurality of busses, each network interface card having a bus interface circuit operatively configured to connect to a respective one of the plurality of busses **(see column 5, lines 15-40, and see column 6, lines 34-40, and see fig. 1).** As shown in fig. 1, there is plurality of modules (14, 16, 18, 20), which has network interfaces for coupling with each other with the 2 buses (10, 12), as shown in fig.1. Status or the first message is being transferred from one module 14 to module 16 periodically. Each module has two identical units such as A0, B0, A1, B1, A2, and B2. Each bus 10 and 12 are connected to both identical unit of each module for redundancy reason;

a memory having a program that periodically transmits a first message to at least one of a plurality of nodes operatively connected to a first of the plurality of busses of the network, determines whether the first message was received by the other of the nodes on the first bus, and transmits a recovery command associated with the first bus to the other of the nodes on a second of the plurality of busses in response to

determining that the first message was not received by the other of the nodes **(see column 6, lines 35-67, and see column 7, lines 1-15, and see fig. 1).** After fault detection, the transmitting module will generate a relevant message to the module again using the 2 buses (10, 12); and

the bus interface circuit including a physical layer controller that sends and receives data on one of the plurality of buses **(Kramer et al. column 5, lines 45-67, column 6, lines 1-20).** Each bus subscribers comprises two controller modules 56-62 for transmitting and receiving data on plurality of buses;

a processing unit for running the program **(see column 1, lines 19-45).** As shown, the system comprises microprocessor, and memory for processing embedded program.

However, Kramer et al. do not teach the recovery command which is configured to cause the other of the nodes to reinitialize a bus interface circuit operatively connected to the other of the nodes to the first bus by commanding; a mean for interrupting power to at least interrupt a current flow from a power bus to a physical layer controller of the bus interface circuit in response to the recovery command; the physical controller to initialize and arbitrate communication on the respective on of the plurality of buses.

Ohyama from the same or similar fields of endeavor teaches the recovery command which is configured to cause the other of the nodes to reinitialize a bus interface circuit operatively connected to the other of the nodes to the first bus by

commanding **(Ohyama see column 4, lines 25-33, fig. 8).** The current detecting circuit shown in fig. 8 can be reset or reinitialize by detecting the OFF state of current flow;

a mean for interrupting power to at least interrupt a current flow from a power bus to a physical layer controller of the bus interface circuit in response to the recovery command **(see column 4, lines 11-15).** The current flowing between L1 and L2 may be interrupted by flickering the switch 19 depending on the On and Off state of a signal, wherein the signal can be the recovery command **(see fig. 4 DCE 7)** DCE is the data circuit terminal or the bus interface circuit **(see fig. 4, DCE 7).** The DCE comprises two ports where the first port or the physical layer controller supplies the L1 signal, and the second port or the link layer controller supplies the L2 signal.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Ohyama in the network of Kramer et al. The motivation for using the feature as taught by Ohyama in the network of Kramer et al. being that it provides reliability in the network.

However, Kramer et al. and Ohyama both do not teach the physical controller configured to initialize and arbitrate communication on the respective on of the plurality of buses.

Fukunaga from the same or similar fields of endeavor teaches the feature of the physical controller to initialize and arbitrate communication on the respective on of the plurality of buses **(Fukunaga et al. paragraph 0245).** The main function of the IC includes bus initialization, arbitration, encoding/decoding.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Fukunaga et al. in the network of Kramer et al. Fee et al. and Ohyama. The motivation for using the feature as taught by Fukunaga et al. in the network of Kramer et al. and Ohyama being that the over-current detection can provide protections to system cause by power outrage.

Regarding claim 33, Kramer et al. disclosed the feature of the second bus is of a different type than the first bus **(Kramer et al. see column 3, lines 15-35).** Since all bus subscribers transmit message independently, the bus are different.

Regarding claim 34, Kramer et al. disclosed the feature of the first message is transmitted once per frame **(Kramer et al. see column 7, lines 49-55).** As shown, all modules are independently and periodically transmitting data to other modules. Therefore we can interpret that each module transmits once in each frame. The frame can be any data packet or message such as status message.

Regarding claim 36, Ohyama disclosed the feature of detecting a current surge in the bus interface circuit of one of the network interface cards; and cycling power to the bus interface circuit of the one network interface card in response to detecting the current surge **(Ohyama see fig. 4, current detecting circuit 15, and column 4, lines 25-33).**

18. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kramer et al. (Pat No.: 6466539), in view of Ohyama (Pat No.: 4794595), and Fukunaga et al.

(Pub No.: 20060002314) as applied to claim 31 above, and further in view of Engels et al. (Pub No.: 2004/0213174).

For claim 35, Kramer et al., Ohyama and Fukunaga et al. disclosed all the subject matter of the claimed invention with the exception of the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame. Engels from the same or similar fields of endeavor teaches the feature of the nodes are operatively configured to transmit a plurality of messages in each of a plurality of frames on the first bus, the first message is one of the plurality of messages, each frame includes a plurality of minor frames, and the first message is transmitted once in each minor frame **(Engels et al. see paragraph 0028, lines 1-4).** The uplink frame, which includes plurality of mini time slot frames, is allocated for data transmission in each individual slot frame. The data can be any kind of messages.

Thus, it would have been obvious to the person of ordinary skill in the art at the time of the invention to use the feature as taught by Engels et al. in the network of Kramer et al. Ohyama and Fukunaga et al. The motivation for using the feature as taught by Engels et al. in the network of Kramer et al. Ohyama and Fukunaga et al. being that the minor frames can be transmitted without major delay.

***Allowable Subject Matter***

Claims 12, 28, 30, and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KAN YUEN whose telephone number is (571)270-1413. The examiner can normally be reached on Monday-Friday 10:00a.m-3:00p.m EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky O. Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Ricky Ngo/
Supervisory Patent Examiner, Art Unit 2616

KY